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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,128	10/15/2003	Kenji Matsushita	10873.1302US01	7371

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EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,128	MATSUSHITA ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-9 and 11* is/are allowed.

6)☒ Claim(s) *1-3,5 and 10* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/12/04, 7/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Preliminary Amendment filed on 15th of October 2003. Claim 10 has been amended; no claim has been canceled; and claim 11 has been newly added. Currently, claims 1-11 are pending in this Application.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-3, 5, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art [hereinafter AAPA] in view of Naohisa et al. [JP 07-334455; cited by the Applicants; hereinafter Naohisa].

Referring to claim 1, AAPA discloses a bus control device (i.e., a conventional bus control device in Fig. 13) comprising

- an external interface (i.e., External Interface 92 of Fig. 13) connected to an external device (i.e., CPU 100 of Fig. 13) via an external system bus (i.e., System Bus 101 of Fig. 13; See page 1, lines 23-24),
- an internal unit (i.e., Internal Unit 93 in Fig. 13),
- a memory interface (i.e., Memory Interface 94 of Fig. 13) connected to an external local memory (i.e., Local Memory 102; See page 1, lines 23-24), and
- an internal bus (i.e., Internal Bus 96 of Fig. 13) at least connecting the external interface (i.e., said External Interface) to the memory interface (i.e., said Memory Interface) and connecting the internal unit (i.e., said Internal Unit) to the memory interface (See page 1, lines 17-19).

AAPA does not teach that the memory interface monitors a usage pattern of the internal bus by the external interface and the internal unit, and sets a priority processing interval that allows only the external interface to use the internal bus in a case where the internal unit is not using the internal bus, thereby prohibiting the internal unit from using the internal bus during the priority processing interval.

Naohisa discloses a bus control module for data transferring (See Fig. 3 and Abstract), wherein a memory interface (i.e., bus control module 1a of Fig. 3)

- monitors a usage pattern (i.e., a busy condition) of an internal bus (i.e., local bus 4 of Fig. 3) by an external interface (i.e., system bus control section 10 of Fig. 3) and an internal unit (i.e., terminal devices 2a-2n in Fig. 3; See paragraph [0009]), and
- sets a priority processing interval (i.e., significant precedence period) that allows only the external interface (i.e., said system bus control section) to use the internal bus (i.e., said local bus) in a case where the internal unit (i.e., said terminal device) is not using the internal bus (i.e., said local bus; See paragraphs [0055]-[0056]),

- thereby prohibiting the internal unit (i.e., said terminal device) from using the internal bus (i.e., said local bus) during the priority processing interval (See paragraphs [0048]-[0052]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said features of said memory interface (i.e., said particular features of bus control module), as disclosed by Naohisa, in said a memory interface (i.e., Memory Interface), as disclosed by AAPA, for the advantage of providing a transfer capability for efficiently performing access to said internal unit (i.e., I/O module) connected to said internal bus (i.e., local bus) from said external system bus (i.e., system bus), and aiming at realizing the data-bus-transfer approach by which the latency times for bus acquisition are reduced (See Naohisa, paragraph [0013]).

However, the recitation in the claim "thereby prohibiting the internal unit from using the internal bus during the priority processing interval" has not been given patentable weight because it has been held that the functional "thereby" statement does not define any structure and accordingly cannot serve to distinguish. *In re Mason, 114 USPQ 127, 44 CCPA 937 (1957).*

Referring to claim 2, AAPA, as modified by Naohisa, teaches the memory interface (i.e., Memory Interface 94 of Fig. 13) comprises

- a bus arbiter (i.e., Bus Arbiter 95 of Fig. 13; AAPA) for arbitrating between a request for use of the internal bus (i.e., Internal Bus 96 of Fig. 13; AAPA) by the external interface (i.e., External Interface 92 of Fig. 3; AAPA) and by the internal unit (i.e., Internal Unit 93 of Fig. 13; See AAPA, page 1, line 36 through page 2, line 7), and
- a priority processing interval managing part (i.e., means for detecting a status of local bus in system bus controller section 10, setting-out register 22, counter 13, comparator 23, and inhibition flag generation part 14 in Fig. 3; Naohisa) for monitoring the usage pattern (i.e., a busy

condition) of the internal bus (i.e., local bus 4 of Fig. 3; Naohisa) based on a result of an arbitration performed by the bus arbiter (i.e., local bus mediation section 12 of Fig. 3; See Naohisa, paragraphs [0044] and [0047]), wherein

- the priority processing interval managing part (i.e., said means for detecting a status of local bus in system bus controller section, setting-out register, counter, comparator, and inhibition flag generation part; Naohisa) notifies the bus arbiter (i.e., said local bus mediation section; Naohisa) and the external interface (i.e., system bus control section 10 of Fig. 3; Naohisa) that only the external interface is permitted to use the internal bus (See Naohisa, paragraph [0055]), in a case where the internal unit (i.e., terminal device 2a-2n in Fig. 3; Naohisa) is not using the internal bus (i.e., said local bus) and sets the priority processing interval (i.e., significant precedence period; See Naohisa, paragraph [0056]), and
- the bus arbiter (i.e., said local bus mediation section) prohibits the internal unit (i.e., said terminal device) from using the internal bus (i.e., said local bus) while the priority processing interval (i.e., significant precedence period) is set (See Naohisa, paragraphs [0047]-[0048]).

Referring to claim 3, Naohisa teaches the memory interface (i.e., bus control module 1a of Fig. 3) comprises

- a priority processing interval setting register (i.e., setting-out register 22 of Fig. 3) for storing information (i.e., setting-out counted value) specifying a length of the priority processing interval (i.e., duration of significant precedence period; See paragraph [0054]), and
- the priority processing interval managing part (i.e., means for detecting a status of local bus in system bus controller section 10, setting-out register 22, counter 13, comparator 23, and

inhibition flag generation part 14 in Fig. 3) sets the priority processing interval (i.e., significant precedence period) based on the information (i.e., said setting-out counted value) stored in the priority processing interval setting register (i.e., said setting-out register; See paragraph [0056]).

Referring to claim 5, Naohisa teaches

- the priority processing interval managing part (i.e., means for detecting a status of local bus in system bus controller section 10, setting-out register 22, counter 13, comparator 23, and inhibition flag generation part 14 in Fig. 3) monitors the usage pattern (i.e., a busy condition) of the internal bus (i.e., local bus 4 of Fig. 3) by confirming the result of the arbitration performed by the bus arbiter (i.e., local bus mediation section 12 of Fig. 3; See paragraphs [0044] and [0047]) at a previously set frequency (i.e., said busy condition of said local bus is monitored by said inhibition flag generation part 14 at every counter-up signal 18 depending on setting-out counted value in setting-out register 22 in Fig. 3; See paragraph [0055]), and
- the frequency (in fact, said setting-out counted value) is set by the external device (i.e., being set by CPU 5 in Fig. 3; See paragraph [0056]).

Referring to claim 10, all of the claim limitations have already been discussed/addressed with respect to claim 1, with the exception of discussing/addressing a CPU connected to the external interface of the bus control device via a system bus, and a local memory connected to the memory interface of the bus control device.

However, the primary reference AAPA further discloses

- a CPU (i.e., CPU 100 of Fig. 13) connected to the external interface (i.e., External Interface 92 of Fig. 13) of the bus control device (i.e., Bus Control Device 91 of Fig. 13) via a system bus (i.e., System Bus 101 of Fig. 13), and

- a local memory (i.e., Local Memory 102 of Fig. 13) connected to the memory interface (i.e., Memory Interface 94 of Fig. 13) of the bus control device (i.e., said Bus Control Device).

Allowable Subject Matter

6. Claims 6-9 and 11 are allowed.

7. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 4, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that the bus arbiter compares a previously set amount of data with the amount of data to be transferred, in a case of receiving a request for use of the internal bus from the internal unit and a notification of the amount of data to be transferred, during the priority processing interval, and when the amount of data to be transferred is equal to or less than the previously set amount of data, the bus arbiter permits the internal unit to use the internal bus during the priority processing interval.

With respect to claim 6 and 10, the claim limitations are respectively deemed allowable over the prior art of record as the prior art fails to teach or suggest that the memory interface prohibits the internal units other than the part of the plurality of internal units, which has a function of dividing data to be transferred to the memory interface via the internal bus and transferring it, from using the internal bus and permits the external interface to use the internal bus, during a period before transfer of all the divided data is completed. The claims 7-9 are dependent claims of the claim 6.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Azevedo et al. [US 6,519,666 B1] disclose arbitration scheme for optimal performance.

Batchelor et al. [US 6,636,913 B1] disclose data length control of access to a data bus.

Shimomura et al. [US 6,333,745 B1] disclose data processor having unified memory architecture providing priority memory access.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

CEL/